In the Claims

1. [Currently Amended] An integrated circuit assembly comprising:

a semiconductive substrate comprising a plurality of field effect transistors having electrically coupled sources and electrically coupled drains comprising regions of the substrate adjacent to a surface of the substrate, and wherein the electrically coupled sources and the electrically coupled drains are collectively configured to conduct power currents in excess of one Ampere; ~~and~~

a package having a plurality of source contacts and a plurality of drain contacts configured to couple with the electrically coupled sources and the electrically coupled drains of the semiconductive substrate, and wherein the source contacts and the drain contacts are provided adjacent to a surface of the package;

at least one metallization layer coupled with the substrate and configured to couple at least some of the sources in parallel and at least some of the drains in parallel; and

wherein the semiconductive substrate further comprises a horizontal interconnect layer formed upon and coupled with the at least one metallization layer, and the horizontal interconnect layer defines a plurality of source contacts and a plurality of drain contacts configured to couple with respective ones of the source contacts and the drain contacts of the package.

2. [Previously Presented] The assembly of claim 1 wherein the semiconductive substrate further comprises a plurality of source contacts and a plurality of drain contacts coupled with respective ones of the sources and the drains of the field effect transistors, and wherein the source contacts and the drain contacts of the package are configured to couple with respective ones of the source contacts and the drain contracts of the semiconductor substrate.

3. Cancel.

4. Cancel.

5. [Original] The assembly of claim 1 wherein the package comprises at least one horizontal interconnect layer to provide the source contacts and the drain contacts.

6. [Original] The assembly of claim 1 wherein all electrical connections intermediate the sources and the drains of the substrate and the source contacts and the drain contacts of the package pass through the surface of the substrate.

7. [Previously Presented] The assembly of claim 1 wherein the package includes one terminal source contact and one terminal drain contact electrically coupled with respective ones of the source contacts and the drain contacts of the package and adapted to electrically couple with devices external

of the integrated circuit assembly.

8. [Original] The assembly of claim 7 wherein the package provides a plurality of electrical paths intermediate the one terminal source contact and the one terminal drain contact and respective ones of the source contacts and the drain contacts of the package, and the electrical paths individually have a resistance less than 1 milliOhm.

9. [Original] The assembly of claim 1 wherein the semiconductive substrate comprises a flip chip semiconductive die.

10. [Previously Presented] The assembly of claim 1 further comprising a plurality of source electrical interconnects and a plurality of drain electrical interconnects coupled with respective ones of the sources and drains and arranged in alternating columns, and wherein the package comprises a plurality of conductive layers corresponding to respective ones of the columns.

11. [Original] The assembly of claim 1 wherein the package comprises at least one horizontal interconnect layer.

12. Cancel.

13. [Previously Presented] The assembly of claim 1 wherein the number of source contacts of the package is less than the number of sources and the number of drain contacts of the package is less than the number of drains.

14. [Original] The assembly of claim 1 wherein the semiconductive substrate comprises a monolithic substrate including the field effect transistors and auxiliary circuitry.

15. [Original] The assembly of claim 1 wherein the semiconductive substrate comprises a monolithic substrate including the field effect transistors and auxiliary circuitry coupled with the plurality of field effect transistors.

16. [Original] The assembly of claim 1 wherein the field effect transistors comprise MOSFET devices.

17. [Currently Amended] An integrated circuit assembly comprising:

a power semiconductor device comprising:

a semiconductive substrate having a surface; and

a power transistor formed using the substrate and having a plurality of source contacts and drain contacts adjacent to and over substantially an entirety of the surface and configured to conduct power currents; ~~and~~

a package having a plurality of source contacts and a plurality of drain

contacts corresponding to and electrically coupled with respective ones of the source contacts and the drain contacts of the power semiconductor device;

at least one metallization layer coupled with the substrate and configured to couple at least some of the source contacts in parallel and at least some of the drain contacts in parallel; and

a horizontal interconnect layer formed upon and coupled with the at least one metallization layer, and the horizontal interconnect layer defines the source contacts and the drain contacts of the power transistor.

18. [Original] The assembly of claim 17 wherein the power transistor comprises a plurality of planar field effect transistors.

19. [Original] The assembly of claim 17 wherein the power transistor comprises a plurality of planar field effect transistors coupled in parallel.

20. Cancel.

21. Cancel.

22. [Original] The assembly of claim 17 wherein the package comprises at least one horizontal interconnect layer to provide the source contacts and the drain contacts of the package.

23. [Original] The assembly of claim 17 wherein all electrical connections intermediate the source contacts and the drain contacts of the substrate and the source contacts and the drain contacts of the package pass through the surface of the substrate.

24. [Original] The assembly of claim 17 wherein the power transistor is configured to conduct power currents in excess of one Ampere.

25. [Original] The assembly of claim 17 wherein the package includes one terminal source contact and one terminal drain contact electrically coupled with respective ones of the source contacts and the drain contacts of the package and adapted to electrically couple with devices external of the semiconductor switching device.

26. [Original] The assembly of claim 25 wherein the package provides a plurality of electrical paths intermediate the one terminal source contact and the one terminal drain contact and respective ones of the source contacts and the drain contacts of the package, and the electrical paths individually have a resistance less than 1 milliOhm.

27. [Original] The assembly of claim 17 wherein the semiconductive substrate comprises a flip chip semiconductive die.

28. [Original] The assembly of claim 17 wherein the source contacts and the drain contacts of the power semiconductor device are arranged in alternating columns, and wherein the package comprises a vertical laminate package comprising a plurality of conductive layers corresponding to respective ones of the columns.

29. [Original] The assembly of claim 17 wherein the package comprises at least one horizontal interconnect layer.

30. [Currently Amended] The assembly of claim 29 wherein the at least one horizontal interconnect layer is spaced from the power semiconductor device; and further comprising a plurality of electrical interconnects intermediate the horizontal interconnect layer of the package and the source contacts and the drain contacts of the power semiconductor device.

31. Canceled.

32. [Previously Presented] The assembly of claim 17 wherein the semiconductive substrate comprises a monolithic substrate including a plurality of field effect transistors and auxiliary circuitry.

33. [Original] The assembly of claim 17 wherein the semiconductive substrate comprises a monolithic substrate including the field effect transistors and auxiliary circuitry coupled with the plurality of field effect transistors.

34. [Original] The assembly of claim 17 wherein the power transistor comprises a plurality of MOSFET devices.

Claims 35-66 have been canceled.

67. [Previously Presented] The assembly of claim 1 further comprising a plurality of source contacts and drain contacts which cover substantially an entirety of the surface of the substrate.

68. [Previously Presented] The assembly of claim 1 further comprising a plurality of source contacts and drain contacts positioned over substantially an entirety of the surface of the substrate.

69. [Previously Presented] The assembly of claim 1 wherein the source contacts and the drain contacts are arranged in a checkerboard pattern.

70. [Previously Presented] The assembly of claim 1 wherein the source contacts and the drain contacts are arranged in a plurality of respective columns.

71. [Previously Presented] The assembly of claim 1 further comprising a plurality of source contacts and drain contacts of the semiconductive substrate and arranged in a plurality of respective columns which extend from one end of the semiconductive substrate to an other end of the semiconductive substrate.

72. [Previously Presented] The assembly of claim 1 wherein the transistors of the semiconductive substrate are configured to conduct currents of about 20 Amperes, or more.

73. [Previously Presented] The assembly of claim 1 wherein the transistors of the semiconductive substrate are configured to conduct currents of about 100 Amperes, or more.

74. [Previously Presented] The assembly of claim 1 wherein the transistors of the semiconductive substrate are configured to conduct currents of about 200 Amperes, or more.

75. [Previously Presented] The assembly of claim 74 wherein the semiconductive substrate has an area of about 4 mm X 4 mm, or less.

76. [Previously Presented] The assembly of claim 75 wherein the source contacts are coupled with a source terminal contact and the drain contacts are coupled with a drain terminal contact, and an on resistance of about 300 microOhms, or less, is provided intermediate the source terminal contact and the drain terminal contact.

77. [Previously Presented] The assembly of claim 1 wherein the source and the drain contacts are individually spaced a substantially uniform distance from adjacent ones of the source and the drain contacts in horizontal and vertical directions.

78. [Previously Presented] The assembly of claim 77 wherein the source and the drain contacts have a pitch of about 250 microns, or less.

79. [Previously Presented] The assembly of claim 77 wherein the source and the drain contacts have a pitch of about 100 microns, or less.

80. [Previously Presented] The assembly of claim 1 wherein the semiconductive substrate supports a plurality of source and drain pads coupled with respective ones of the sources and the drains and having a pad pitch of less than or equal to about 40 microns in one of vertical and horizontal directions of the source and drain pads.

81. [Previously Presented] The assembly of claim 80 wherein the semiconductive substrate supports an intermediate layer configured to electrically couple the source and drain pads with the source contacts and the drain contacts of the package.

82. Cancel.

83. [Previously Presented] The assembly of claim 10 wherein the conductive layers are individually electrically coupled with more than one of the electrical interconnects.

84. [Previously Presented] The assembly of claim 1 wherein the package includes one terminal source contact and one terminal drain contact electrically coupled with respective ones of the source contacts and the drain contacts, and an electrical path intermediate the one terminal source contact and the one terminal drain contact has a resistance of 300 microOhms, or less.

85. [Previously Presented] The assembly of claim 84 wherein the electrical path is configured to conduct currents in the range of 100-200 Amperes.

86. [New] The assembly of claim 1 wherein the horizontal interconnect layer comprises a copper plane.

87. [New] The assembly of claim 1 wherein the horizontal interconnect layer permits usage of a plurality of pads defined by the at least one metallization layer having an increased density compared with a denisty of the source contacts and the drain contacts of the package.

88. [New] An integrated circuit assembly comprising:

a semiconductive substrate comprising a plurality of field effect transistors having electrically coupled sources and electrically coupled drains comprising regions of the substrate adjacent to a surface of the substrate, and wherein the electrically coupled sources and the electrically coupled drains are collectively configured to conduct power currents in excess of one Ampere;

a package having a plurality of source contacts and a plurality of drain contacts configured to couple with the electrically coupled sources and the electrically coupled drains of the semiconductive substrate, and wherein the source contacts and the drain contacts are provided adjacent to a surface of the package; and

a plurality of source electrical interconnects and a plurality of drain electrical interconnects coupled with respective ones of the sources and drains and arranged in alternating columns, and wherein the package comprises a

vertical laminate package comprising a plurality of conductive layers corresponding to respective ones of the columns.

89. [New] An integrated circuit assembly comprising:

a semiconductive substrate comprising a plurality of field effect transistors having electrically coupled sources and electrically coupled drains comprising regions of the substrate adjacent to a surface of the substrate, and wherein the electrically coupled sources and the electrically coupled drains are collectively configured to conduct power currents in excess of one Ampere;

a package having a plurality of source contacts and a plurality of drain contacts configured to couple with the electrically coupled sources and the electrically coupled drains of the semiconductive substrate, and wherein the source contacts and the drain contacts are provided adjacent to a surface of the package; and

wherein the source contacts and the drain contacts are arranged in a checkerboard pattern.